IN THE CLAIMS:

Claims 1-6 have been amended herein. All of the pending claims 1 through 6 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Currently Amended) A method of forming a semiconductor device package, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, ~~said~~the active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of ~~said~~the plurality of individual die locations;

forming intermediate conductive elements over ~~said~~the plurality of bond pads to project a height above ~~said~~the active surface;

forming a pattern of mutually transverse channels in ~~said~~the active surface to a depth below ~~said~~the at least one layer of integrated circuitry, ~~said~~the channels circumscribing a semiconductor ~~element~~ device location comprised of at least one individual die and exposing peripheral edges of ~~said~~the at least one layer of integrated circuitry;

applying an encapsulant material at least over ~~said~~the active surface and into ~~said~~the channels to a depth exceeding ~~said~~the height of projection of ~~said~~the intermediate conductive elements;

removing a depth of ~~said~~the encapsulant material sufficient to expose a portion of each of ~~said~~the intermediate conductive elements; and

placing ~~said~~the semiconductor substrate with ~~said~~the intermediate conductive elements in alignment with conductive bumps protruding from a carrier substrate; and

electrically connecting ~~said~~the intermediate conductive elements and ~~said~~the conductive bumps.

2. (Currently Amended) The method of claim 1, further including forming bond pads over the exposed portions of ~~said~~the intermediate conductive elements before electrically connecting ~~said~~the intermediate conductive elements to ~~said~~the conductive bumps.

3. (Currently Amended) A method of forming a semiconductor device package, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, ~~said~~the active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of ~~said~~the plurality of individual die locations;

forming intermediate conductive elements over ~~said~~the plurality of bond pads to project a height above ~~said~~the active surface;

forming a pattern of mutually transverse channels in ~~said~~the active surface to a depth below ~~said~~the at least one layer of integrated circuitry, ~~said~~the channels circumscribing a semiconductor ~~element~~ device location comprised of at least one individual die and exposing peripheral edges of ~~said~~the at least one layer of integrated circuitry;

applying an encapsulant material at least over ~~said~~the active surface and into ~~said~~the channels to a depth exceeding ~~said~~the height of projection of ~~said~~the intermediate conductive elements;

removing a depth of ~~said~~the encapsulant material sufficient to expose a portion of each of ~~said~~the intermediate conductive elements; and

forming conductive traces over ~~said~~the encapsulant material from ~~said~~the exposed portions of ~~said~~the intermediate conductive elements to at least one channel of ~~said~~the pattern of channels, defining a peripheral edge of at least one individual die location of ~~said~~the plurality so as to define a plurality of laterally spaced edge contacts therealong, and severing ~~said~~the semiconductor substrate in alignment with at least some of ~~said~~the channels including ~~said~~the at least one channel into a plurality of semiconductor elements each comprised of ~~said~~the at least one individual die location, wherein ~~said~~the exposed

peripheral edges of ~~said~~the at least one layer of integrated circuitry remain covered with ~~said~~the encapsulant material and ~~said~~the plurality of laterally spaced edge contacts are located along a peripheral edge of a semiconductor element of the plurality.

4. (Currently Amended) The method of claim 3, further comprising aligning ~~said~~the plurality of laterally spaced edge contacts with a plurality of edge connectors of a carrier substrate and electrically connecting the plurality of laterally spaced edge contacts with the plurality of edge connectors.

5. (Currently Amended) A method of forming a semiconductor device package, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, ~~said~~the active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of ~~said~~the plurality of individual die locations;

forming intermediate conductive elements over ~~said~~the plurality of bond pads to project to a peripheral edge of at least one individual die location of ~~said~~the plurality so as to define a plurality of laterally spaced edge contacts therealong;

forming a pattern of mutually transverse channels in ~~said~~the active surface to a depth below ~~said~~the at least one layer of integrated circuitry, ~~said~~the channels circumscribing ~~said~~the at least one individual die location and exposing ~~said~~the laterally spaced edge contacts of ~~said~~the peripheral edge;

applying an encapsulant material at least over ~~said~~the active surface and into ~~said~~the channels to a depth ~~exceeding said height of projection of said~~ covering the intermediate conductive elements; and

severing ~~said~~the semiconductor substrate in alignment with at least some of ~~said~~the channels ~~including said at least one channel~~ into a plurality of semiconductor elements each comprised of ~~said~~the at least one individual die location, wherein ~~said~~the plurality of

laterally spaced edge contacts are exposed along the peripheral edge of ~~said~~ the at least one individual die location.

6. (Currently Amended) The method of claim 5, further comprising aligning ~~said~~the plurality of laterally spaced edge contacts with a plurality of edge connectors of a carrier substrate and electrically connecting the plurality of laterally spaced edge contacts with the plurality of edge connectors.